A COMPACT MODEL FOR SILICON CONTROLLED RECTIFIERS IN LOW VOLTAGE CMOS PROCESSES

BY

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THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2014

Urbana, Illinois

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ABSTRACT

This thesis presents an SCR compact model for simulating ESD protection circuits. The aspects of the compact model that are necessary to reproduce measurement data, such as quasi-static I-V curves and transient voltage overshoot, are discussed. These aspects include conductivity modulation of the well resistances in the SCR, impact ionization at the N-well/P-well junction, and the influence of electric fields in the well region on carrier diffusion between the anode and cathode. Further, a detailed validation of the compact model is presented. A methodology for parameter extraction is also discussed.

ACKNOWLEDGMENTS

I would like to that my advisor, Professor Elyse Rosenbaum for helping me improve as a scientist and communicator.

I would like to thank several current and former students in my research group for their teaching, helpful discussion, and advice that helped me to prepare this thesis. Nathan Jack, Kuo-Hsuan Meng, Vrashank Shukla, Nick Thomson, and Min-Sun Keel, thank you for your help.

I would like to thank my friends and family for all their support.

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CHAPTER 1

INTRODUCTION

Electrostatic discharge (ESD) is one of several common causes of failure of integrated circuits (ICs) [1]. Prior to an ESD event, a static charge is stored on some insulated object; if the insulated object is subsequently grounded, the accumulated charge will rapidly discharge. Static charges can accumulate on the assembled ICs through their storage containers, or on the people handling the ICs due to their clothing contacting the environment. While these sparks may be a simple nuisance to people, the microscopic devices used on modern ICs experience ESD as a potentially damaging electric current. Though ESD events typically only last between 1 ns and 1 μs, the peak current of an ESD event is generally on the order of several amperes; however particularly severe ESD events may approach ten amperes. In order to successfully manufacture a modern IC, ESD must be carefully managed both in factory and on-chip.

An on-chip ESD protection network is designed to limit on-chip voltages, currents and powers within a safe range of values during an ESD event, while having minimal adverse impact on the chip's normal operation. Because the protection network should not affect the chip's normal operation, it is usually designed as a network of high current (physically large compared to other on-chip devices) switches which are off except during an ESD event. Diodes, BJTs, MOSFETs, and silicon controlled rectifiers (SCRs) are all commonly used as switches in ESD protection networks. During an ESD event, a well-designed switching network can provide a low impedance path between any two points where ESD current may enter/leave the chip. By providing a deliberate low impedance path, the switching network both limits the voltages across sensitive devices and shunts current away from the fragile functional circuitry of the chip.

Unfortunately, standard simulation models for possible switches often become inaccurate at high currents, even though the physical devices they represent can survive such conditions during a brief ESD event. This creates the dilemma that the ESD designer must (a) design without reliable simulation data, (b) make the switches large enough so they never reach high current operation, or (c) use a specialized high current simulation model. Option (a) is unappealing because it does not allow the design to be verified without being manufactured; manufacturing in the semiconductor industry is often a slow and expensive enough process to make a "trial and error" approach unacceptable. Similarly, option (b) is unappealing because it

wastes chip area, which is one of the dominant costs associated with chip manufacturing. Therefore, the designer's best choice is option (c), which requires a specialized high current simulation model.

The remainder of this thesis will discuss high current simulation models for SCRs in low voltage CMOS processes. Chapter 2 provides additional background information on low voltage CMOS SCRs. In Chapter 3, a new simulation model is presented and briefly compared to prior art. Chapter 4 verifies the new simulation model by comparing measurements and simulation. Chapter 5 presents a parameter extraction procedure for the model. Chapter 6 draws conclusions and suggests potential future work.

CHAPTER 2

SCR BACKGROUND

The SCR is a semiconductor device formed by three back-to-back P-N junctions, resulting in a P-N-P-N structure. A cross-section of an SCR in a low voltage CMOS process is shown in Figure 2.1. In Figure 2.1, SCR's P-N-P-N structure is formed by the anode, N-well, P-well, and cathode. For the remainder of this thesis, these terminals will be referred to as A, NW, PW, and C, respectively.

An SCR's behavior is best understood by treating it as a pair of cross-coupled bipolar transistors: an NPN with emitter, base, and collector corresponding to C, PW, and NW, and a PNP with emitter, base and collector corresponding to A, NW, and PW. A schematic of these cross-coupled bipolar transistors is shown in Figure 2.2(a). To understand how an SCR works, it is instructive to look at a circuit that uses an SCR, such as the diode-triggered SCR (DTSCR) [2] shown in Figure 2.2(b). For the DTSCR in Figure 2.2(b), as long as V_{SCR} is below four diode drops (the on-voltage of a diode), corresponding to the PNP's emitter-base junction and the diode string, the PNP will be in cutoff mode; the NPN's base is connected to its emitter, so it will be in cutoff mode, too. However, if V_{SCR} is raised above four diode drops, the PNP transistor will enter forward active mode, and its collector current will begin to flow out of the PW terminal. If the PNP's collector current is large enough so that the voltage drop across the PW's series resistance is one diode drop, the PNP's collector current will begin to flow across the NPN's base-emitter junction and the NPN will enter forward active mode, and its collector

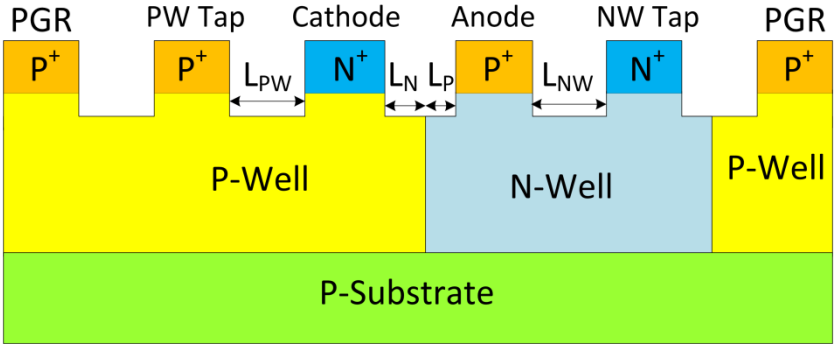


Figure 2.1: Cross-section of an SCR in a low voltage CMOS process. P-well and N-well are abbreviated PW and NW respectively. The terminal labeled PGR represents a P-type guard ring that surrounds the entire SCR, which will generally be shorted to the cathode. In circuit implementations where the P-well tap is grounded, the P-guard ring may be merged with the P-well tap. Critical device dimensions are also labeled.

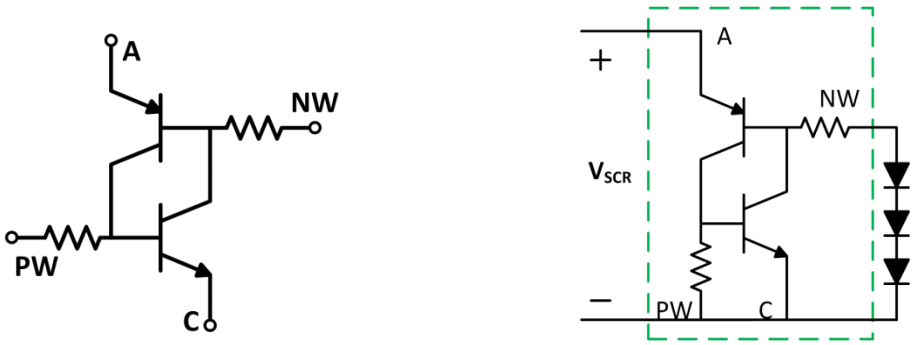


Figure 2.2: Circuit representation of an SCR. Only the cross-coupled bipolar transistor representation of an SCR is shown in (a), which is drawn with a series resistance for the PW and NW terminals to represent contact resistance and the resistance of the P- and N-wells. A sample SCR circuit, the diode-triggered SCR (DTSCR) is shown in (b), where the SCR is surrounded with a dashed line.

current will flow through the PNP's base-emitter junction. Provided that both transistors have high enough current gain, they will drive each other into saturation, which will cause the SCR to conduct higher current at a lower voltage. This behavior is called snapback. In this state, the total voltage across the SCR is the sum of V_{CEsat} of the NPN and $V_{EB(on)}$ of the PNP, a total of about 0.9 V. It is also possible to activate the SCR by forcing current into the NPN's base, instead of the PNP, and such a configuration will behave very similarly.

The simplified discussion of SCR operation presented above neglects resistive voltage drops in the SCR. In addition to the total 0.9 V drop across the three P-N junctions, two more types of voltage drops play an important role in SCRs at high currents. First, because the A and C terminals (the emitters of the PNP and NPN transistors) can conduct a large amount of current, their series resistance can cause a significant voltage drop that is linear with the current. Second, when either the NPN or PNP transistor is at a high current, the majority and minority carrier concentrations (both of which are roughly proportional to emitter current) at the edge of the base-emitter junction will increase beyond the background doping concentration. If both transistors are at high current, the average hole and electron gradients between the N-well/anode junction and the P-well/cathode junction will be small, so the diffusion current will be fairly small; the current across this region must be caused by drift. Since, as mentioned earlier, the carrier concentration in this region is proportional to the current, the resistance across this region is inversely proportional to the current across it; at high currents, the voltage drop across this region will be constant because, as the current increases, the resistance decreases.

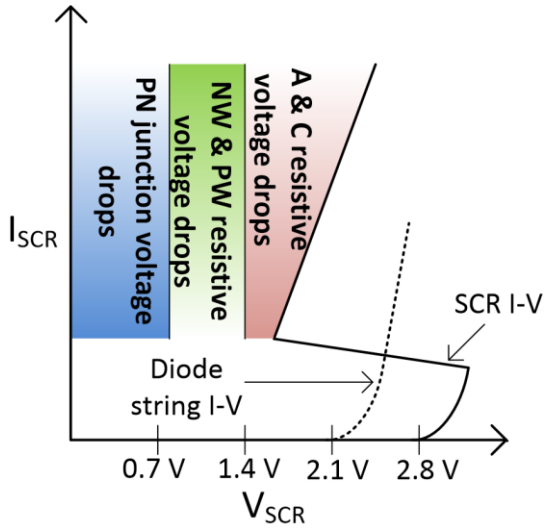


Figure 2.3: Conceptual I-V curve of a DTSCR, such as that shown in Figure 2.2. The off-state (low current) I-V is determined primarily by the diode string. The on-state (high current) I-V is determined by the SCR.

At currents below snapback, the behavior of an SCR can be predicted by treating the SCR as independently operating bipolar transistors. At currents above snapback, the two resistive terms discussed in the previous paragraph and the voltage drop across the P-N junctions determine the I-V characteristics. By combining the I-V curve branches before and after snapback, an SCR circuit's I-V curve can be drawn, as shown in Figure 2.3 for the DTSCR presented in Figure 2.2(b).

Two of the most promising SCR compact models available in the ESD literature are presented in [3] and [4, 5]. The model presented in [3] uses a two-part representation of an SCR. In the off-state, the SCR is modeled as a pair of cross-coupled bipolar transistors by using an Ebers-Moll representation. In the on-state, a PIN diode-like representation is used which correctly represents the drift dominated current conduction in an on-state SCR. However, the discontinuity caused by switching between these two states can lead to convergence problems. The model described in [4, 5] represents an SCR as two cross-coupled bipolar transistors using a set of modified Gummel-Poon equations. However, this model connects both of the collector resistors directly to their respective well contacts, where they cannot contribute to the voltage drop between the anode and cathode, as shown in Figure 2.4. In order to reproduce the on-branch of a measured I-V curve, the model must reverse bias the N-well/P-well junction, which disagrees with the generally accepted description of SCR operation given at the beginning of this chapter. Furthermore, since the model uses the diffusion-based Gummel-Poon model to represent the SCR's on-state current, which is dominated by drift, the model requires highly empirical

extensions which increase its parameter extraction burden. The model presented in Chapter 3 is continuous while providing a physically accurate description of the voltage drops between the anode and cathode.

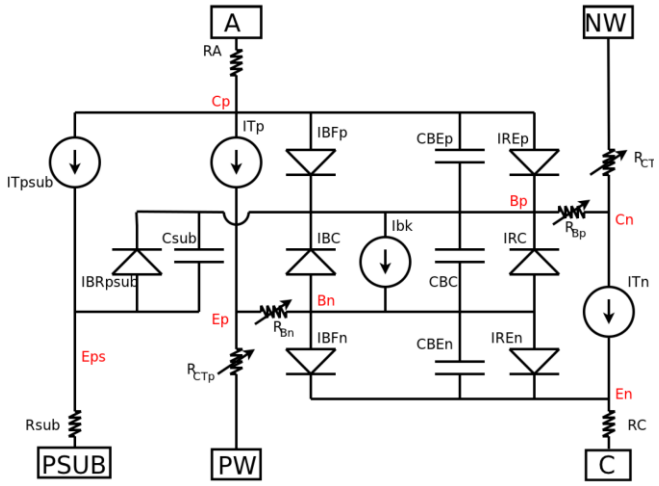


Figure 2.4: Schematic representation of the SCR compact model in [4, 5]. The voltage drop between the anode and cathode is comprised of only two components: the resistive drop associated with the anode/cathode terminals and the voltage drop across the three PN junctions. In order to account for the resistive voltage drop associated with the NW/PW, the NW/PW junction must be erroneously reverse biased.

CHAPTER 3

SCR COMPACT MODEL

A schematic representation of the model is provided in Figure 3.1. It includes cross-coupled NPN and PNP transistors. Each transistor uses a modified Ebers-Moll model and includes non-linear junction and diffusion capacitances, non-linear base and collector resistances, and avalanche current across the N-well/P-well junction. The emitters (anode and cathode in Figure 3.1) have the highest current densities and therefore the highest Joule heating. The increased differential resistance of SCRs at high currents is captured by modeling the emitter resistors as explicit functions of temperature; self-heating of and thermal diffusion away from these regions is modeled using a first-order RC thermal equivalent circuit [3, 6]. The model equations are summarized in Table 3.1. The model parameters are listed in Table 3.2. The model parameters are expressed as functions of the layout geometry in Table 3.3, and the scaling parameters used in Table 3.3 are described in Table 3.4. This model has been implemented in Verilog-A and simulated using Spectre.

The placement of the collector resistors, $R_{C,N}$ and $R_{C,P}$, within the SCR model schematic of Figure 3.1 allows voltage drops due to drift current in the N-well/P-well regions to contribute to the total voltage drop between the anode and cathode. This is a novel feature of the model presented in this thesis. Although $R_{C,N}$ and $R_{C,P}$ have a significant impact on the SCR holding voltage, they contribute relatively little to the device on-resistance; the collector resistance is inversely proportional to the current due to conductivity modulation, resulting in a near constant voltage drop through these elements.

The unique orientation of the collector resistors in Figure 3.1 has another benefit: holding voltage scaling with regard to well-tap spacing can be modeled from first principles. Changing the well tap spacings changes the base resistances; this will change the balance of current between the NW/PW junction and one or the other base resistance, depending on the trigger circuit implementation, thereby modulating the holding voltage via differences in conductivity modulation of the collector resistors. Previous models [3, 4, 5] reproduce this behavior empirically.

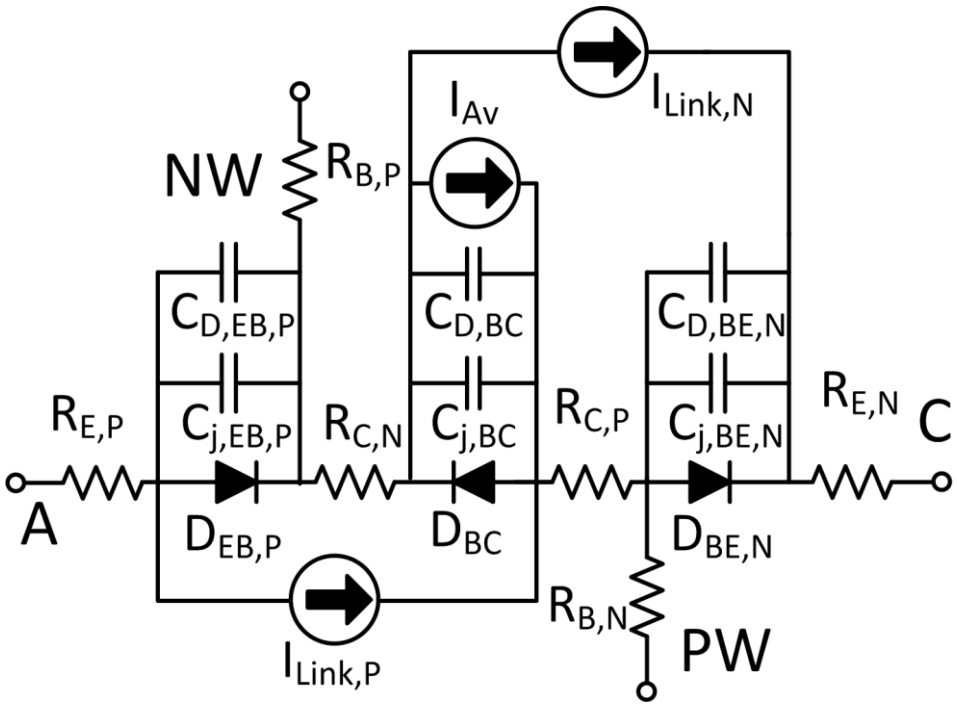


Figure 3.1: Circuit representation of the model. Components associated with the NPN and PNP are labeled with "N" and "P," respectively. Components associated with the shared bases/collectors created by the NW/PW junction are labeled with "BC." The potential drop between the A and C terminals has three components: diodes drops, resistive drops across the conductivity modulated collector resistances, and ohmic drops across the emitter resistances.

Table 3.1: Selected equations for the SCR model. Ebers-Moll equations are used for the NPN and PNP transistors. For each NPN equation marked with (*), there is a corresponding PNP equation (not shown). Each junction capacitor (C_j) is modeled using the expression marked with (**). Impact ionization current (I_{Av}) is modeled using the Miller multiplication expression. The P term in the self-heating equation (second from the bottom) represents the sum of the current-voltage products for $R_{E,N}$ and $R_{E,P}$.

$I_{Link,N} = \boldsymbol{I_{SN}}\left[exp\left(\frac{V_{BE,N}}{V_T}\right) - exp\left(\frac{V_{BC,N}}{V_T}\right)\right]*$	$I_{D,BE,N} = \frac{\boldsymbol{I_{SN}}}{\beta_{FN}}\left[exp\left(\frac{V_{BE,N}}{V_T}\right) - 1\right]*$
$\beta_{FN} = \boldsymbol{\beta_{N0}} + \frac{I_{Link,P}}{\boldsymbol{I_{\beta P}}}\left(\frac{1}{1+\frac{I_{Link,P}}{\boldsymbol{I_{\beta PSat}}}}\right)*$	$Q_{D,BE,N} = \boldsymbol{I_{SN}\tau_{FN}}\left[exp\left(\frac{V_{BE,N}}{V_T}\right) - 1\right]*$
$I_{D,BC} = \boldsymbol{I_{SR}}\left[exp\left(\frac{V_{BC}}{V_T}\right) - 1\right]$	$Q_{D,BC} = \boldsymbol{I_{SR}\tau_R}\left[exp\left(\frac{V_{BC}}{V_T}\right) - 1\right]$
$R_{\mathrm{B,N}} = \boldsymbol{R_{B,Nmin}} + \frac{\boldsymbol{R_{\mathrm{B,N0}}} - \boldsymbol{R_{B,Nmin}}}{1+\frac{Q_{D,\mathrm{BE,N}}}{\boldsymbol{Q_{\mathrm{B,N0}}}}}*$	$R_{C,N} = \frac{\boldsymbol{R_{C,N0}}}{1+\frac{Q_{D,BC}}{\boldsymbol{Q_{C,N0}}}}*$
$R_{\mathrm{E,N}} = \boldsymbol{R_{E,N0}}\left(1+\frac{\Delta T}{T_0}\right)^{\chi}*$	$P = \mathbf{C_{th}}\frac{d(\Delta T)}{dt} + \frac{\Delta T}{\boldsymbol{R_{th}}}$
$I_{Av} = (\boldsymbol{I_{SR}} + I_{Link,N} + I_{Link,P})\left(\frac{1}{1-\left(\frac{V_{Av}}{\boldsymbol{BV_R}}\right)^{\boldsymbol{m_R}}} - 1\right)$	$\mathrm{C_j} = \frac{\boldsymbol{C_{j0}}}{\left(1-\frac{V_j}{\boldsymbol{\varphi}}\right)^{\boldsymbol{m_j}}}**$

Table 3.2: Parameters list for the model described in Table 3.1.

Parameters	Description
I_{SN}, I_{SP}, I_{SR}	NPN, PNP, and reverse saturation currents
τ_{FN}, τ_{FP}, τ_{R}	NPN, PNP, and reverse transit times
β_{N0}, β_{P0}	NPN and PNP common emitter current gains
$I_{\beta P}$, $I_{\beta N}$	NPN and PNP mutual current gain parameters
$I_{\beta PSat}$, $I_{\beta NSat}$	NPN and PNP mutual current gain saturation parameters
$C_{j0,BE,N}$, $m_{j,BE,N}$, $\phi_{BE,N}$, $C_{j0,EB,P}$, $m_{j,EB,P}$, $\phi_{EB,P}$, $C_{j0,BC}$, $m_{j,BC}$, ϕ_{BC}	Junction capacitance parameters
BV_{R}, m_{R}	N-well/P-well impact ionization parameters
$R_{E,N0}$, $R_{B,Nmin}$, $R_{E,P0}$, $R_{B,Pmin}$	Emitter and base contact resistances
$R_{C,N0}$, $R_{C,P0}$, $R_{B,N0}$, $R_{B,P0}$	Zero conductivity modulation collector/base silicon resistances
$Q_{C,N0}$, $Q_{C,P0}$, $Q_{B,N0}$, $Q_{B,P0}$	Collector/base conductivity modulation charges
R_{th}, C_{th}, χ	Self-heating parameters

The equations for β_N and β_P in Table 3.1 differ from those in the Ebers-Moll model by allowing the link current (I_{Link} in Figure 3.1) of one transistor to influence the current gain of the other. This modification is necessary because the base of one of the BJTs in the SCR overlaps with the collector of the other, and vice versa. A majority carrier current flowing through the collector of one transistor will induce an electric field in the base of the other transistor, as illustrated in Figure 3.2 for the case of a diode-triggered SCR (DTSCR). The electric field induced in the base aids minority carrier transport in this region and, consequently, augments the current gain. It should be noted that there is no experimental evidence that justifies the specific form given for β_N and β_P in Table 3.1; instead, experiment only suggests that, in some devices, the current gain of both the NPN and PNP, when measured separately, are below 1 at currents just above those required for snapback. Without a mechanism that increases the current gain through the interaction of the transistors, snapback is theoretically impossible (though it is observed) in the majority of the low voltage CMOS devices considered; therefore, there must be such a mechanism. However, this current gain increase only occurs during the SCR's on-state, so this effect is impossible to measure directly.

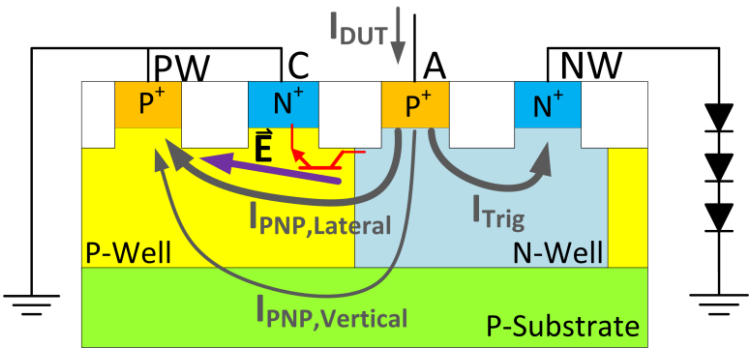


Figure 3.2: The lateral portion of the PNP's collector current induces an electric field in the NPN transistor's base which aids electron transport across this region, thereby increasing the current gain of the NPN transistor. $I_{PNP,Lateral}$ and $I_{PNP,Vertical}$ represent the link currents of the PNP transistor that leave the well laterally and vertically, respectively.

Conductivity modulation in the base resistors, $R_{B,N}$ and $R_{B,P}$, plays an important role in determining the peak voltage across an SCR as it turns on. Before the SCR is latched on, the base-emitter junction of one transistor and an external trigger circuit provide a current path that limits the voltage across the SCR. However, there is a time lag before the base resistors reach their final, conductivity-modulated values and these resistances will not reach their steady-state values during the fast rising edge of a CDM-like event. This is one of the most important sources of SCR overshoot. The formulation of base resistance in this thesis is similar to that in [4].

Although the collector resistors $R_{C,N}$ and $R_{C,P}$ also undergo conductivity modulation, the equations used to model the collector resistors are slightly different from those used to represent the base resistors $R_{B,N}$ and $R_{B,P}$. As indicated in Table 3.1, the base resistors include a minimum resistance value, whereas the collector resistors do not. The minimum resistance values for the base resistors represent the contact resistance of the associated well tap. Since the collector resistors are contained completely within the silicon, there is no associated contact resistance.

Each model parameter is split into two parts: one that is associated with the horizontal, drawn dimensions and another that is associated with the fixed vertical dimensions of the technology in question (e.g. shallow trench isolation, or STI, depth). The drawn dimensions are labeled in Figure 2.1. For example, $R_{C,N}$ can be separated into a horizontal component associated with L_P and a vertical component associated with the distance between the anode diffusion and the bottom of the adjacent STI. As indicated in Table 3.3, many of the model parameters are represented as linear functions of one or another drawn dimension. This approach yields a simple geometric interpretation of the scaling equations and provides adequate accuracy.

Table 3.3: Geometric scaling equations. Model parameters are bolded in this table and described in Table 3.4. Critical dimensions are shown in Figure 2.1. Parameters I_{SN}, I_{SP}, I_{SR}, $I_{\beta N}$, $I_{\beta P}$, $I_{\beta Nsat}$, $I_{\beta Psat}$ and the C_{j0} parameters, which are not listed in the table, scale linearly with width. All other parameters do not vary with geometry. The $R_{BN,0}$ equation in this table is specific to an N-well triggered device.

$\tau_{FN} = \boldsymbol{P_1}(\boldsymbol{L_1} + L_N)^{n_1}$	$\tau_{FP} = \boldsymbol{P_2}(\boldsymbol{L_2} + L_P)^{n_2}$	$\tau_R = \boldsymbol{P_3}(\boldsymbol{L_3} + L_N + L_P)^{n_3}$
$\beta_{N0} = \boldsymbol{K_1}\left(2L_N - \boldsymbol{L_{N,min}}\right)^{-n_4}$	$\beta_{P0} = \boldsymbol{K_2}\left(2L_P - \boldsymbol{L_{P,min}}\right)^{-n_5}$	
$R_{C,N0} = \dfrac{\boldsymbol{A_1} + \boldsymbol{B_1}L_P}{W}$	$R_{C,P0} = \dfrac{\boldsymbol{A_2} + \boldsymbol{B_2}L_N}{W}$	
$\dfrac{1}{R_{B,N0}} = \dfrac{W}{\boldsymbol{A_3} + \boldsymbol{B_3}L_{PW}} + \dfrac{W}{\boldsymbol{A_4} + \boldsymbol{B_4}L_{NW}}$	$R_{B,P0} = \dfrac{\boldsymbol{A_5} + \boldsymbol{B_5}L_{NW}}{W}$	
$Q_{C,N0} = (\boldsymbol{C_1} + \boldsymbol{D_1}L_P) \cdot W$	$Q_{B,N0} = (\boldsymbol{C_3} + \boldsymbol{D_3}L_{PW}) \cdot W$	
$Q_{C,P0} = (\boldsymbol{C_2} + \boldsymbol{D_2}L_N) \cdot W$	$Q_{B,P0} = (\boldsymbol{C_4} + \boldsymbol{D_4}L_{NW}) \cdot W$	

Table 3.4: Parameter list for the geometric scaling model in Table 3.3. Parameters n_1, n_2 and n_3 are restricted to values between 1 and 2. A value near 1 indicates that drift is the dominant means of transport, while a value near 2 indicates that diffusion is dominant.

Parameters	Description
P_1, P_2, P_3	Transit time coefficient
n_1, n_2, n_3	Transit time exponent
L_1, L_2, L_3	Vertical transport distances
K_1, K_2, n_4, n_5, $L_{N,min}$, $L_{P,min}$	Empirical fitting parameters for β scaling
A_1, A_2, A_3, A_4, A_5	Vertical components of resistances
B_1, B_2, B_3, B_4, B_5	Horizontal components of resistances
C_1, C_2, C_3, C_4	Vertical components of conductivity modulation charges
D_1, D_2, D_3, D_4	Horizontal components of conductivity modulation charges

The parameters that have a non-linear dependence on the drawn dimensions are the transit times τ_{FN}, τ_{FP}, and τ_R, the current gains β_{N0} and β_{P0}, and the NPN base resistance $R_{B,N}$. Each transit time is modeled as a power law function of the relevant drawn dimension, with an exponent between 1 and 2 [3]. This model is justified by observing that both drift and diffusion contribute to charge flow in the well regions, with transit times that are linearly and quadratically proportional to path length, respectively. It is well known that the current gain β is not a linear function of base width [7]; this parameter is modeled using a simplified version of the scaling equation presented in [3].

As seen in Table 3.3, $R_{B,P0}$ is a simple, linear function of the N-well tap spacing L_{NW}, while $R_{B,N0}$ is represented as a function of both L_{PW} and L_{NW}; this is a result of the device being built atop a P-type substrate. Figure 3.3 illustrates the resistive network through which the hole current may flow. First, consider the case of an N-well triggered SCR (e.g., DTSCR); the trigger circuit current ($I_{Trig,NWT}$) flows directly from the anode to the N-well tap and the resulting PNP link current ($I_{Link,NWT}$) flows to the node labeled "B_{NPN}." From this point, it will flow through R_{C-PW}, R_{C-PGR}, and the P-well/cathode junction. The PW and PGR terminals are shorted together by metal interconnects, allowing the resistance R_{PW-PGR} to be ignored. R_{C-PW} is a linear function of L_{PW} and R_{C-PGR} is a linear function of L_{NW}; the two resistors are in parallel, resulting in a net resistance that depends on both L_{PW} and L_{NW}. This is the specific case modeled by the equation for $R_{B,N0}$ in Table 3.3. Next, consider the case of a P-well triggered device; current injected into the P-well tap by the trigger circuit will flow through a path involving all three P-type resistors shown in Figure 3.3, plus the cathode/P-well junction; therefore, the model for $R_{B,N0}$ must contain all three resistive elements. Furthermore, R_{C-PW} is the only one of the three resistors that will undergo significant conductivity modulation. Thus, in the case of a P-well triggered SCR, $R_{B,N}$ represents R_{C-PW}, which should be modeled using the equation for $R_{B,N}$ in Table 3.1. R_{C-PGR} and R_{PW-PGR} of the P-well triggered SCR are not present in the model as shown in Figure 3.1; they should be modeled as constant resistances. The proposed representation of the substrate network for the P-well triggered SCR has not been rigorously validated experimentally, though the base resistance scaling trends presented in Chapter 4 suggest that this representation is reasonable.

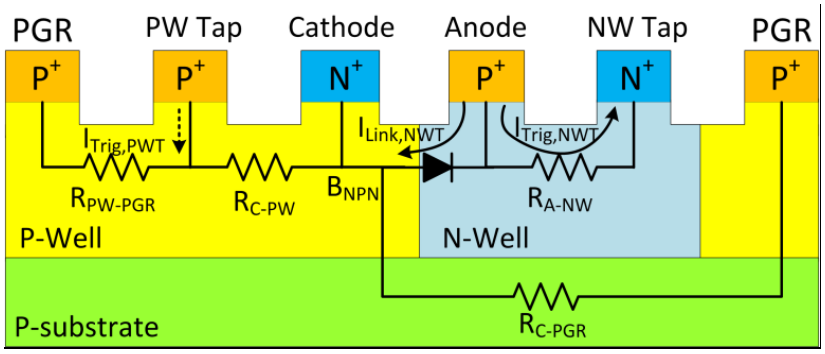


Figure 3.3: Substrate resistance network in a CMOS SCR. For N-well triggered devices, the PW and PGR terminals are both tied to the cathode, and the SCR latches on when the P-well/cathode junction is forward biased due to $I_{Link,NWT}$, which denotes the PNP link current for an N-well triggered device. Both R_{C-PW} (proportional to L_{PW}) and R_{C-PGR} (proportional to L_{NW}) determine the resistance between node B_{NPN} and the metal connecting the PGR, PW tap, and cathode. In contrast, for a P-well triggered device with trigger current $I_{Trig,PWT}$, R_{PW-PRG} contributes to the base resistance of the NPN since it is not strapped to the PW tap.

Several aspects of this model are non-trivial to implement; in these cases, a poor implementation can lead to a simulation model that does may not converge. Specifically, these relationships are the equations given for impact ionization (I_{Av} in Table 3.1), junction capacitance (C_j in Table 3.1), and the equations for variable current gain.

Impact ionization is very well predicted by the Miller multiplication expression (see I_{Av} in Table 3.1). However, two well-recognized issues prevent it from being used in simulation [8]-[11]: (1) it has a singularity at the breakdown voltage so the simulator may attempt to divide by zero, and (2) it is inaccurate above the breakdown voltage—due to discrete time steps, the simulator may give a non-physical, but mathematically correct, output, in which the voltage across the junction in question is greater than the breakdown voltage. To avoid these problems, Equation (3.1) is substituted for the I_{Av} equation in Table 3.1 whenever V_{Av} exceeds $k \cdot BV_R$, where k is a number slightly smaller than 1, e.g. 0.999,

$$I_{Av} = \left(I_{SR} + I_{Link,N} + I_{Link,P}\right)\left(\frac{1}{1-k^{m_R}} - 1 + \frac{V_{Av} - k \cdot BV_R}{V_k}\right). \tag{3.1}$$

This is equivalent to replacing the branch labeled I_{Av} in Figure 3.1 with a differential resistance of value

$$r_{Av} = \frac{V_k}{I_{SR} + I_{Link,N} + I_{Link,P}}. \tag{3.2}$$

The parameter V_k, which controls the value of the differential resistance near the breakdown voltage, should be made small enough such that the voltage across the junction cannot exceed the breakdown voltage. This can be ensured by placing a constraint on V_k, e.g.,

$$\frac{V_k}{I_{SR}} < 0.05\ \Omega. \tag{3.3}$$

The equations used to model the junction capacitances contain a similar singularity; however, in the voltage ranges where the junction capacitance equation is numerically problematic, diffusion capacitance typically dominates. In light of this observation, it is common to place a maximum limit on the value of the junction capacitance, e.g., $2C_{j0}$ [12], or one may use the technique in [13] to remove the singularity.

When using the relationship for β_N and β_P from Table 3.1, the model shows generally robust convergence; problems were encountered in only approximately 1% of simulations of TLP

pulses. Complete elimination of convergence problems in N-well triggered SCRs was achievable by setting either β_P to a small fixed value (≈0.5) or β_N to a large fixed value (≈5). This is acceptable if the model will be used with only a single triggering topology (i.e., N-well or P-well triggering); otherwise, the parameters will need to be re-extracted when the triggering mechanism is changed. Another possible alternative would be to develop a different relationship for the current gain with better convergence properties. As discussed on page 9, experimental evidence only suggests that current gain increases during snapback; there is no evidence for any particular functional form of this increase.

CHAPTER 4

COMPACT MODEL VALIDATION

Quasi-static I-V data and transient V(t) data were obtained from TLP and VFTLP measurement of SCR test structures fabricated in 65 nm and 130 nm CMOS technologies. VFTLP measurements were performed using 10 ns wide pulses with 300 ps rise time. The voltage waveform is measured using a high impedance probe placed at the device anode. Inverse filtering of the waveform is performed to compensate for the band-limited probe [14]. The steady-state current is calculated using a TDR-O framework using measurements from a CT-1 current probe. TLP measurements were performed using Kelvin probing. The measurement data are compared to data obtained from circuit simulation in order to evaluate the compact model.

First compared are the measured and simulated turn-on responses of a 65 nm DTSCR to VFTLP. The voltage across the device V(t) is plotted in Figure 4.1(a); the simulations correctly show that the turn-on time varies with the amplitude of the incident pulse or, equivalently, with the steady-state current. In Figure 4.1(b), the peak voltage during device turn-on is plotted as a function of the steady-state current. The peak voltage is predicted correctly by simulation only when impact ionization at the N-well/P-well junction is included in the model (I_{Av} in Figure 3.1/Table 3.1). A failure to include impact ionization will prevent the model from accurately modeling overshoot at high currents. Furthermore, because the link currents, $I_{Link,P}$ and $I_{Link,N}$, build up over time, failure to include impact ionization induced multiplication of the link currents (e.g. [4, 5]) will prevent the model from capturing the rise-time dependence of the overshoot voltage. As the rise-time of the ESD pulse increases, the link currents have more time to build up toward their steady-state values, providing a larger seed current for impact ionization, thereby allowing for better voltage clamping. For completeness, the pulsed I-V curves are shown in Figure 4.1(c).

Next, the current gain model is validated. Figure 4.2 shows the measured, pulsed I-V characteristic of a 65 nm DTSCR. Also plotted are two I-V curves from simulation. In one simulation, the current gain parameter $ß_{FN}$ was fixed at its measured value $ß_{N0}$; the value of $ß_{N0}$ was obtained by characterizing the three-terminal NPN. In the other simulation, $ß_{FN}$ was non-constant, as given by the model in Table 3.1. Simulation results match the measurement results

only when the model of Table 3.1 is used, in which $ß_{FN}$ is a function of the PNP link current, $I_{Link,P}$. The measurement data suggest $R_{on} \approx 0$ near the holding point; this is attributed to non-uniform conduction across the device width [15], which existing models—[3-5] and this thesis—do not replicate. However, strong agreement in this region is not critical; the challenge in designing SCR circuits is ensuring the peak transient voltage and steady-state voltage/current current and voltages are limited to safe values. In this region, these quantities are all relatively small.

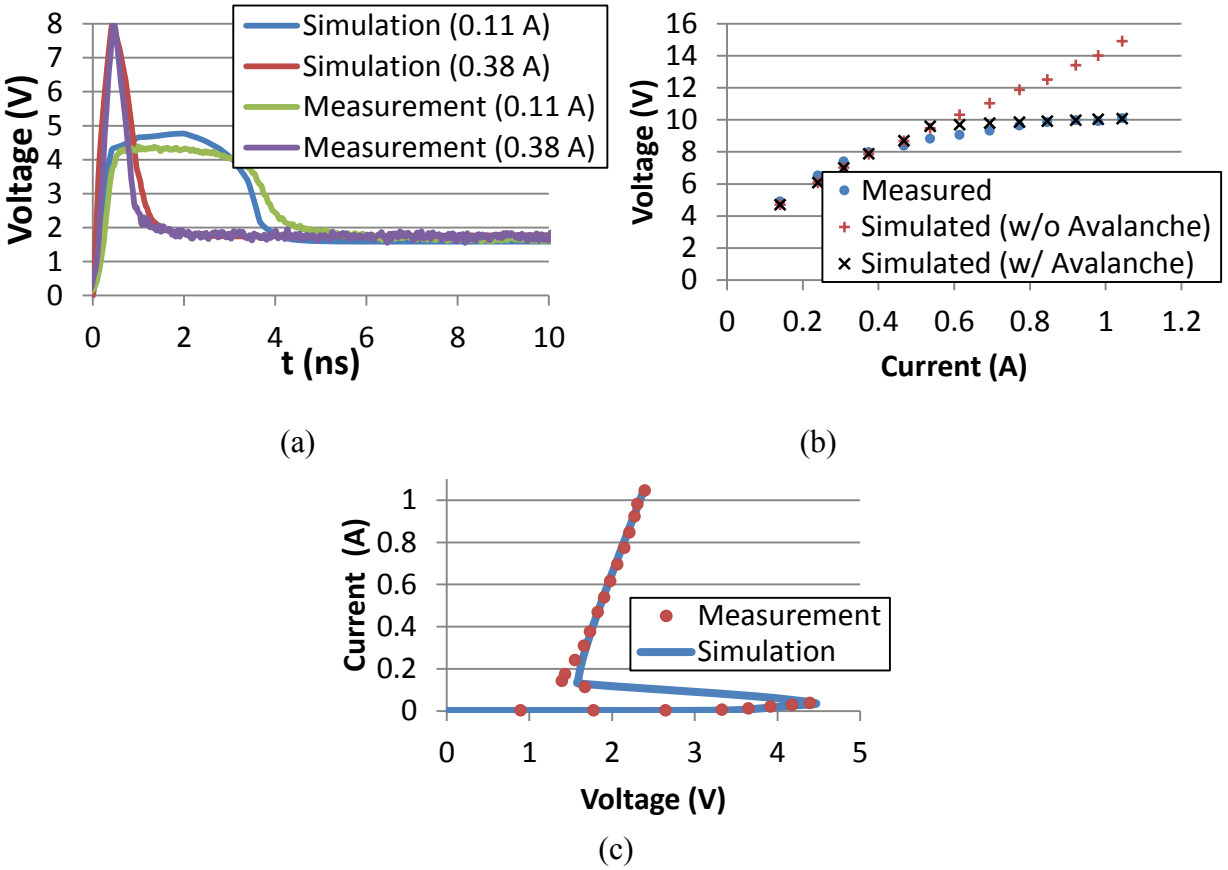


Figure 4.1: Measured and simulated pulse response for a DTSCR in 65 nm CMOS (t_{rise} = 300 ps, t_{width} = 10 ns). Plot (a) shows the transient responses at steady-state currents of 0.11 A (1.5 mA/µm) and 0.38 A (5 mA/µm). Plot (b) shows the peak voltage observed as a function of the steady-state current; simulation is performed with and without N-well/P-well avalanching modeled. $V_{peak} > dc\text{-}V_{t1}$ is observed due to the pulse's short rise time. Plot (c) shows the pulsed I-V characteristic for the device. The device's drawn dimensions are {W = 75 µm, $L_P + L_N$ = 0.3 µm, L_{PW} = 5 µm, L_{NW} = 5 µm}.

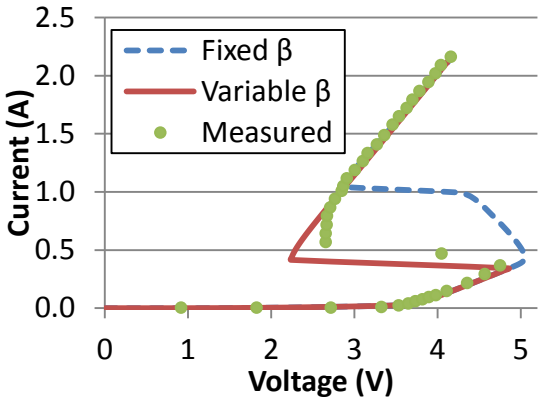


Figure 4.2: Measured and simulated I-V curves for a DTSCR in 65 nm CMOS. Using the measured β_{N0} of the three-terminal NPN yields a poor fit where both transistors are active, i.e. the negative differential resistance region. The device's dimensions are {W = 150 µm, $L_P + L_N$ = 0.3 µm, L_{PW} = 0.3 µm, L_{NW} = 0.3 µm}.

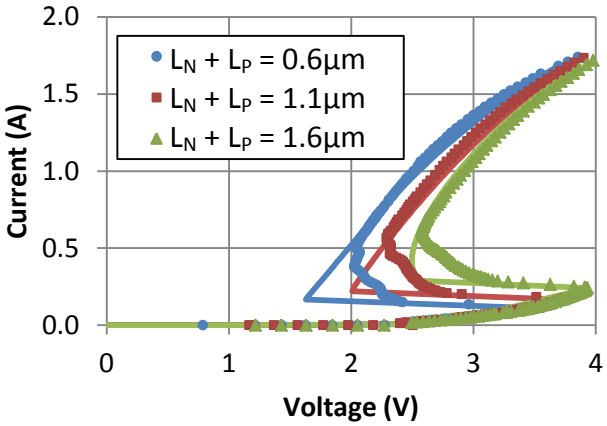


Figure 4.3: Measured and simulated pulsed I-V characteristics of DTSCRs in a 130 nm CMOS process. The device width is 50 µm. Devices have varying anode to cathode spacing. L_{PW} and L_{NW} are fixed at 0.22 µm. The measurement data were originally presented in [3].

Finally, the ability of the model to capture the effects of the variable layout spacings is evaluated. In Figure 4.3, the measured, pulsed I-V characteristics of 130 nm DTSCRs with varying anode-to-cathode spacing ($L_N + L_P$) are plotted, along with the corresponding simulation results. The model is observed to well represent the dependence of I_{t1} and V_{Hold} on anode-to-cathode spacing. As in Figure 4.2, there some disagreement between measurement and simulation near the holding point; however, in Figure 4.3 the discrepancy likely has a different root cause. A typical TLP measurement setup does not produce a pulse with a perfectly flat top, so increasing the voltage will change the time during the pulse at which snapback occurs. Since the plotted I-V points are a time average of the current/voltage, the measurement data show a gradual transition between the high and low impedance states. However, the simulated applied pulses are much

more ideal, so the variation in snapback time does not appear, resulting in a much sharper transition between the high and low impedance states. As argued on page 16, this disagreement is of little consequence. The collector resistance parameters $R_{C,P0}$ and $R_{C,N0}$, the current gain parameters β_{N0} and β_{P0}, and the charge storage parameters τ_R and Q_{C0} all vary with this dimension. Figure 4.4 demonstrates that all of these parameters are appropriately modeled by the equations in Table 3.3; more specifically, R_{C0} (Figure 4.4(a)) and Q_{C0} (Figure 4.4(b)) are shown to scale linearly with anode-cathode spacing, while τ_R (Figure 4.4(c)) is shown to require a higher order function.

Figure 4.5 demonstrates that the model reproduces the dependency of V_{Hold} and I_{t1} on well-tap spacing. This behavior is captured by varying only the base resistance parameters, as discussed in Chapter 3. There is some disagreement near the holding point; it is caused by the same process that causes the disagreement in Figure 4.3. Figure 4.6 shows how $R_{B,N}$ and $R_{B,P}$ vary with each well tap spacing. $R_{B,P}$ is observed to be only a function of the anode/N-well tap spacing,

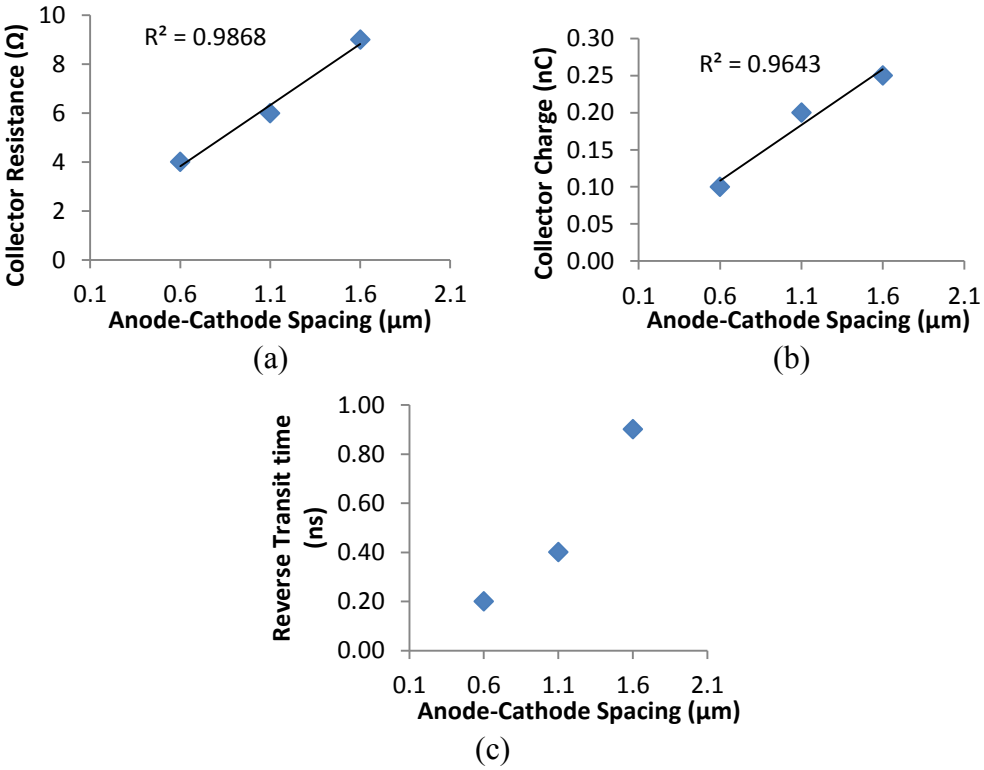


Figure 4.4: Scaling behavior with respect to anode-cathode spacing for (a) collector resistance, R_{C0}, (b) collector charge, Q_{C0}, and (c) reverse transit time, τ_R. To simplify parameter extraction, the NPN and PNP are assumed to have identical R_{C0} and Q_{C0}. Parameters are determined by minimizing the error in overshoot and quasi-static I-V characteristics.

consistent with the equation for $R_{B,P0}$ given in Table 3.3. $R_{B,N}$, however, is a function of both the anode/N-well tap spacing and the cathode/P-well tap spacing, again consistent with the model equations of Table 3.3, and confirming that the resistance of the substrate below the N-well does play a significant role in determining SCR behavior (e.g. I_{t1}).

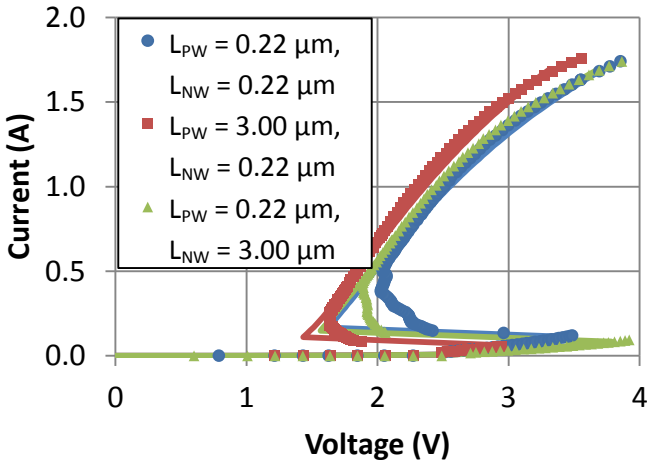


Figure 4.5: Measured and simulated pulsed I-V characteristics of DTSCRs in a 130 nm CMOS process. The device width is 50 µm. Anode to cathode spacing ($L_N + L_P$) is fixed at 0.6 µm. L_{PW} and L_{NW} vary as shown in the legend. The measurement data were originally presented in [3].

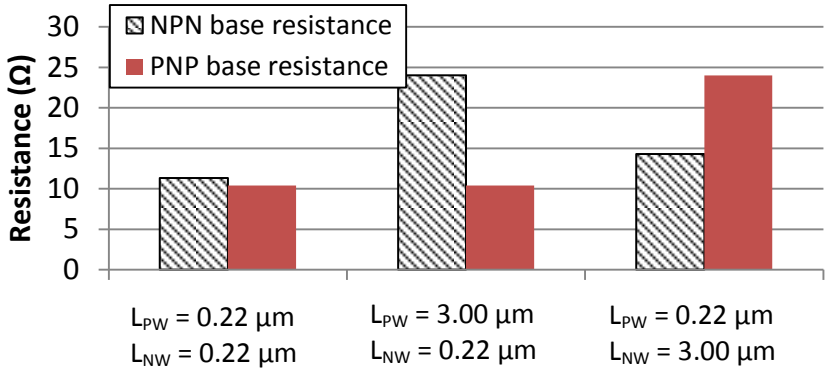


Figure 4.6: Base resistances as a function of well tap spacing for the same DTSCRs as in Figure 4.5. Increasing L_{PW} only changes $R_{B,N}$, whereas increasing L_{NW} increases both $R_{B,N}$ and $R_{B,P}$.

CHAPTER 5

PARAMETER EXTRACTION PROCEDURE

Many of the parameters used for this model can be measured directly. These include the saturation currents (I_{SN}, I_{SP}, and I_{SR}) and junction capacitance parameters (C_{j0}, m_j and φ for each junction), and the Miller multiplication parameters for the NW-PW junction (BV_R and m_R). Measurement procedures for each of these parameters are discussed in this chapter. Some or all of these parameters may also be available from a PDK. In particular, the capacitance parameters should be taken from the PDK; the junction capacitance has only a minor effect on an SCR's transient behavior and direct measurement would require either additional s-parameter test structures or large area test structures for use with an LCR meter. Obtaining values for each of these parameters is the first step of the extraction procedure.

The saturation currents (I_{SN}, I_{SP}, and I_{SR}) are determined from the I-V characteristics of the NPN and PNP transistors inherent in the SCR, and are measured using a semiconductor parameter analyzer. Either three-terminal BJT structures or four-terminal SCR structures are required. For this measurement, the collector and base should be grounded and the emitter voltage should be swept from 0 V to about 1 V [-1 V] for a PNP [NPN] transistor. Typical measurement data are shown in Figure 5.1. If the P^+-diffusion [N^+] is used as the emitter, extrapolating the linear section of $\log(I_C)$ to the current axis gives I_{SP} [I_{SN}]. If the PW or NW is used as the emitter, extrapolating the linear section of $\log(I_B)$ to the current axis gives I_{SR}. The value of β (= I_C/I_B) measured here should only be used with caution, as the current gain will likely be significantly reduced under ESD-like conditions.

The Miller multiplication parameters can be determined by using a semiconductor parameter analyzer to measure the I-V characteristics of either the NPN or PNP transistors that compose an SCR, so either a three-terminal BJT structure or a four-terminal SCR structure is required. I_C should be swept in linear steps at several values of I_B, including $I_B = 0$. Example raw measurement data from a PMOS in 130 nm CMOS is shown in Figure 5.2(a). Each I-V curve should be post-processed to generate a plot like the one in Figure 5.2(b), which can then be matched to the analytic model. The post-processing should use Equation (5.1),

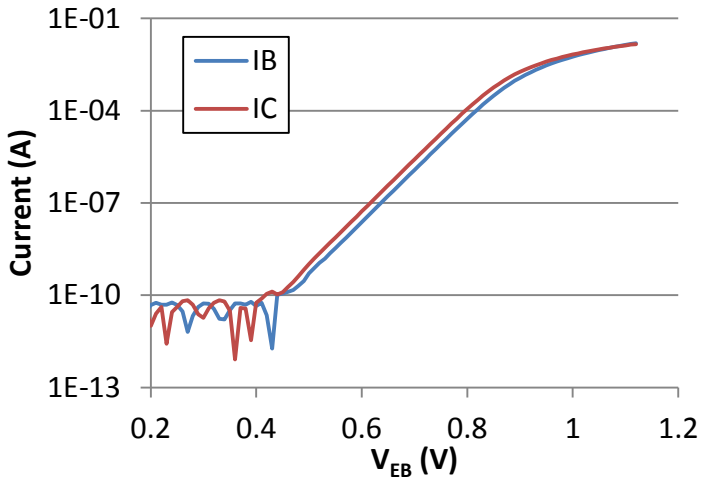
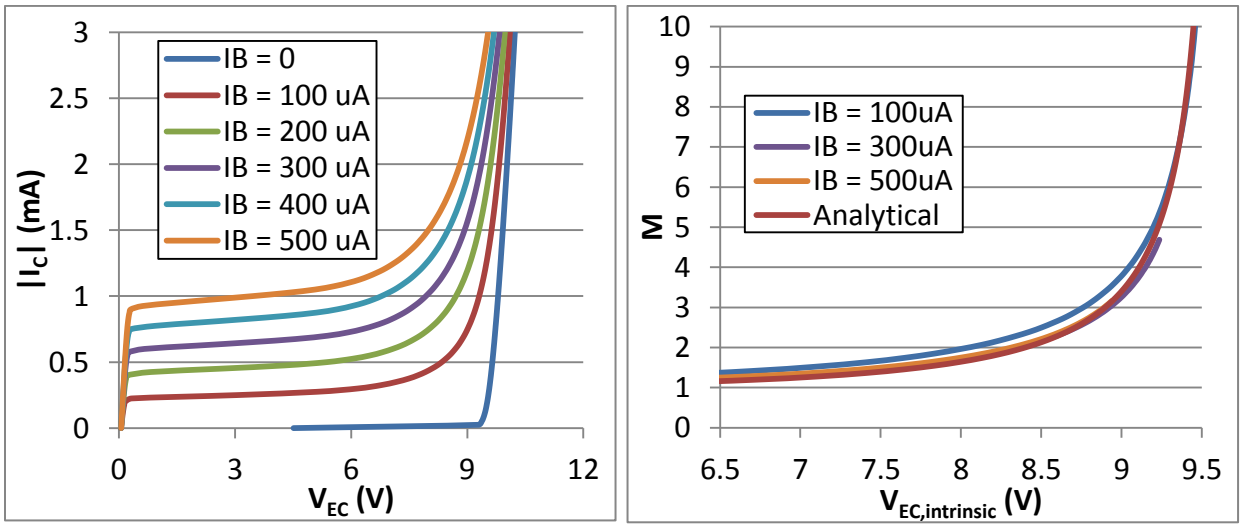


Figure 5.1: Measured I_B and I_C vs. V_{EB} of a PNP transistor in 130 nm CMOS. At low V_{EB}, the noise floor prevents direct measurement of the I_S parameters.

$$R_{on} = \frac{dV_{EC}}{dI_C}, \quad V_{EC,intrinsic} = V_{EC} - I_C R_{on}, \quad M = \frac{I_C}{I_{CSAT}}, \tag{5.1}$$

where R_{on} should be evaluated using the $I_B = 0$ curve at high currents, and I_{CSAT} should be a measured collector current with $V_{EC} \approx 1.5$ V. Because this method requires a value for I_{CSAT}, the $I_B = 0$ curve (where the transistor is in cutoff mode prior to avalanche) will not give a reliable estimate of M. Note that the Miller multiplication expression uses the base-collector voltage so the base-emitter voltage must be subtracted from $V_{EC,intrinsic}$ when matching the M curve.



(a) (b)

Figure 5.2: Example plots of the extraction procedure for Miller multiplication parameters, including (a) the raw measurement data and (b) extracted $M(V_{EC})$ curve.

The remaining parameters are best determined with the aid of an optimizer that attempts to match simulated and measured maximum voltage values during turn-on and quasi-DC I-V characteristics. This process can be aided by using good initial estimates of parameters.

Reasonable initial estimates of the τ_F parameters may be obtained from two-port S-parameter measurements of each bipolar transistor, biased in the common emitter configuration [3]; the small-signal base-emitter capacitance under various bias conditions is used to calculate τ_F. The final, best-fit values will generally be smaller than those obtained from this measurement because the SCR operates at higher current levels than can be used for S-parameter measurements. As an example, the best-fit parameters used in [16] were $[\tau_{FN}, \tau_{FP}]$ = [75 ps,110 ps] respectively, which are approximately half the measured transit time of structures with identical cross-section [3]. Similarly, an initial guess for β_0 can be obtained from three-terminal DC measurements; however, the extracted β_0 will be too large because the current levels are higher under ESD conditions. Note that τ_R can be estimated in a similar way to τ_{FP} and τ_{FN}, but the error will likely be larger.

Similarly, reasonable estimates of $R_{B,N0}$, $R_{B,P0}$, $Q_{B,N0}$, $Q_{B,P0}$, $R_{E,N}$, $R_{E,P}$ can be obtained from DC measurements performed on stand-alone bipolar structures, as shown in Figure 5.3. Note that in order to determine Q_B, the values of τ_F and β that will be used in the model must be known due to the formulation of R_B, which is presented here in a different (but equivalent) form than in Table 3.1:

$$R_B = R_{B,min} + \frac{R_{B,0} - R_{B,min}}{1 + \frac{I_B}{I_{B0}}}, \quad I_{B0} = \frac{Q_{B0}}{\beta_F \tau_F}. \tag{5.2}$$

Using Equation (5.2), $R_{B,min}$, $R_{B,0}$, and I_{B0} should be extracted to optimize the match to the measured $R_B(I_B)$. This equivalent formulation is more convenient for parameter extraction than the original formulation from Table 3.1 since it directly relates the resistance to the terminal currents. In contrast, the original formulation requires the final values for β_F and τ_F (which have not yet been determined) to obtain a similar relationship. Caution should be used when using the R_B model obtained through this measurement method; in a P-well triggered SCR (e.g. GGSCR [17]), the NPN base resistance network could be significantly different in the stand-alone test structure and the SCR due to the presence of guard rings, such as shown in Figure 3.3. As such, for P-well triggered SCRs, any stand-alone test structures should not include a guard ring if this

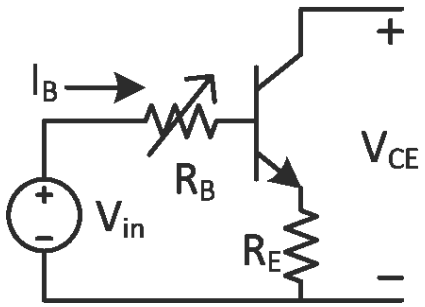


Figure 5.3: Measurement technique for estimating R_B and R_E [18]. The collector current is set to 0, V_{in} is swept from 0 to ≈1.1 V, and V_{CE} is measured. The voltage drop between the collector and emitter has three terms: V_{BE}, V_{BC}, and the voltage across R_E. At high currents, V_{BE} and V_{BC} are weak functions of I_B, so R_E becomes the only significant contributor to $\frac{dV_{CE}}{dI_B}$. $R_B(I_B)$ can be determined from the bias conditions, the now known value of R_E and assuming that V_{BE} is constant.

measurement method is going to be used. However, for an N-well triggered SCR, (e.g. DTSCR [2]), the base of one transistor is connected to its emitter in the SCR circuit, the low-current base resistance should be used as this configuration establishes an electric field profile that inhibits conductivity modulation in the base resistance; in this case, the base resistance is best extracted by matching I_{T1} to the TLP I-V curve.

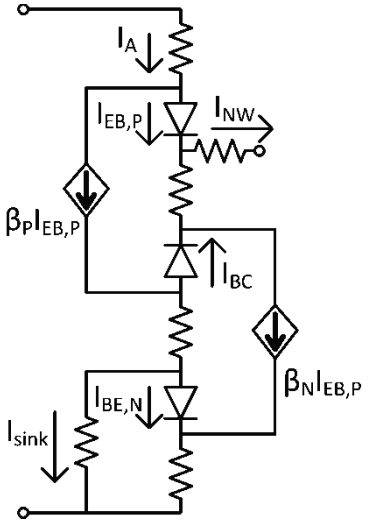
Unlike the base/emitter resistances, there is no good method for obtaining a measured estimate of R_{C0} and Q_{C0}. Instead, coarse estimates should be obtained for R_{C0} and Q_{C0} from the PDK sheet resistance values. By treating the collector region as a uniformly doped rectangular volume of silicon with total free charge Q_{C0} and assuming a specific value for the carrier mobility, μ, Q_{C0} can be estimated from the collector geometry and sheet resistance using

$$Q_{C0} = \frac{W \cdot L}{\mu R_S}. \tag{5.3}$$

These parameters will be primarily determined by the optimizer.

The I_β and $I_{\beta Sat}$ parameter values cannot be measured and thus must be estimated (and later optimized using a parameter optimizer using the method discussed below); initial values should be selected to constrain β to two values; when only one transistor is on, β should be β_0 in that transistor; when both transistors are on, β should reach a fixed value above 3. Practically, this means that $I_{\beta Sat}$ will be several times smaller than I_{t1}. Setting the parameters to ensure these conditions are met is beneficial for three reasons: (1) the resulting model will yield an on-state I-V curve that matches measurement well, (2) the voltage drop in the wells is weakly dependent on current so it is physically reasonable that the current gain be modeled as constant in the on-state,

and (3) enforcing the constraint of a nearly constant β makes it easier to develop analytic equations for the model's I-V behavior, which can be used as constraining equations for parameter extraction. For example, by assuming constant β and $I_{NW} = 0$ (as in an NW triggered SCR in the on-state, where the NW is connected to the trigger circuit, which does not conduct in the on-state), all of the branch currents can be calculated in terms of the anode current with good precision, as shown in Figure 5.4. The formula shown for I_{sink} can be derived by assuming that the NPN's base-emitter voltage ($V_{BE,N}$) is a constant, V_{on}, and that R_{BN} is constant (which in this case is a good assumption, as the electric field will inhibit conductivity modulation in the silicon represented by R_{BN}). Because all of the branch currents are known, the $I_A(V_A)$ can be easily written in terms of model parameters, though the full representation is rather lengthy.



$$I_{EB,P} = \frac{1}{1+\beta_P} I_A$$

$$I_{BE,N} = \frac{1}{1+\beta_N} (I_A - I_{sink})$$

$$I_{BC} = \frac{\beta_N \beta_P - 1}{(1+\beta_N)(1+\beta_P)} I_A - \frac{\beta_N}{1+\beta_N} I_{sink}$$

$$I_{sink} \approx \frac{(1+\beta_N) R_{EN} I_A + V_{on}}{R_{BN} + (1+\beta_N) R_{EN}}$$

Figure 5.4: Schematic and resulting branch currents for an on-state NW triggered SCR from KCL equations. By using the branch currents and model equations, accurate analytic equations for the on-state I-V can be obtained.

The methods described above provide a way of estimating all of the parameters except for those associated with self-heating. As such, it is now practical to use an optimizer to match the measured and simulated transient (especially peak voltage) and quasi-DC characteristics. Because no estimate of the self-heating parameters has been obtained thus far, it is recommended that the optimization be performed first using VFTLP transients. The self-heating parameters can then be extracted and optimized based on 100 ns TLP transients, as was done in [6].

Special care must be taken to obtain accurate transient data. High impedance probes commonly used for measuring TLP voltage waveforms will filter the waveform. Measured waveforms must be post-processed to remove this filtering. The transfer function of the probe

may be estimated from transient measurements using the method presented in [19], or an S-parameter based measurement technique could be used.

An error in one SCR parameter value may be compensated by an error in the trigger circuit model; thus, the optimization should be performed using at least two different trigger circuits to avoid any such hidden errors. The two trigger circuits should inject current into the same well. Furthermore, the optimization should be performed for both N-well and P-well triggered devices, requiring four total test structures for a single SCR layout geometry. This parameter extraction procedure is used to obtain a general purpose SCR model; if only a single SCR/trigger-circuit combination is to be modeled, the optimization need not be so comprehensive.

Parameter optimization algorithms are widely studied and are not problem specific, so they will not be discussed here; however, the cost function to be optimized is problem specific and the implementation can be non-trivial. One meaningful cost function, F, for a set of parameters, X, with m data points taken at n rise times on several devices is

$$F(X) = \sum_{devices}\left(\sum_{m}\left(V_{QS,sim}(I,X) - V_{QS}(I)\right)^2 + \frac{\alpha}{n}\sum_{n}\left(\frac{1}{m}\sum_{m}\left(V_{peak,sim}(I,X,t_{r,n}) - V_{peak}(I,t_{r,n})\right)^2\right)\right). \quad (5.4)$$

The current, I, is taken to be the quasi-static value, even when evaluating $V_{peak}(I)$. The parameter α denotes the relative importance of the fit of the quasi-static I-V and the peak transient voltage as a function of current. Larger values of α will give higher weight to the peak overshoot data. Because the measurement data and simulation data must be taken at discrete points, exact values of for the functions $V_{peak,sim}$ and V_{peak}, and $V_{QS,sim}$ and V_{QS} (the quasi-static voltages) will not be available at the same current. In order to evaluate F as given above, it is necessary to interpolate between each data point of the measured data. Practically, this interpolation can be done using the sorted (in order of increasing quasi-static current) set of measured I-V points. Then, for example, $V(I_0)$ can be evaluated using linear interpolation between the two I-V points with current immediately greater than and less than I_0.

CHAPTER 6

CONCLUSION

The layout scalable SCR compact model presented in this thesis is a significant improvement over prior art. By including the effect of several important physical behaviors, excellent agreement with measurement is obtained. These newly included physical behaviors include conductivity modulation of the well-taps, impact ionization based multiplication of diffusion currents across the PW-NW junction, and conductivity modulation of the well-regions between the anode and cathode. The two former behaviors are required to accurately reproduce the peak voltage seen across the SCR during fast transients, whereas the latter is required to reproduce the quasi-steady-state I-V curve. Since all of these behaviors are accurately represented, it is possible to use this compact model to perform optimization of SCR behavior using circuit simulation, though this is beyond the scope of this thesis.

REFERENCES

[1] K. T. Kaschani and R. Gaertner, "The impact of electrical overstress on the design, handling and application of integrated circuits," in *Proc. EOS/ESD Symp*., 2011.

[2] M. Mergens et al., "Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides," in *Proc. IEEE Int. Electron Devices Meeting*, 2003, pp. 515-518.

[3] J. Di Sarro and E. Rosenbaum, "A scalable SCR compact model for ESD circuit simulation," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3275–3286, Dec. 2010.

[4] A. Romanescu et al., "A novel physical model for the SCR ESD protection device," in *Proc. EOS/ESD Symp*., 2010, pp. 21-30.

[5] A. Romanescu et al., "Scalable modeling studies on the SCR ESD protection device," in *Proc. EOS/ESD Symp*., 2011, pp. 179-186.

[6] J. Li, S. Joshi, R. Barnes, and E. Rosenbaum, "Compact modeling of onchip ESD protection devices using Verilog-A," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst*., vol. 25, no. 6, pp. 1047–1063, Jun. 2006.

[7] Y. Taur and T. Ning, *Fundamentals of Modern VLSI Devices,* 2nd ed. New York: Cambridge Univ. Press, 2009, p. 334.

[8] C. Diaz and S.-M. Kang, "New algorithms for circuit simulation of device breakdown," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst*., vol. 11, no. 11, pp. 1344-1354, Nov. 1992.

[9] S. G. Beebe. "Simulation of complete CMOS I/O circuit response to CDM stress," in *Proc. EOS/ESD Symp.*, 1998, pp. 259-270.

[10] M. Mergens et al., "Modular approach of a high current MOS compact model for circuit-level ESD simulation including transient gate coupling behavior," in *Proc. IEEE Int. Rel. Phys. Symp*, 1999, pp. 167-178.

[11] S. Joshi and E. Rosenbaum, "Compact modeling of vertical ESD protection NPN transistors for RF circuits," in *Proc. EOS/ESD Symp*., 2002, pp. 292-298.

[12] P. Grey, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integred Circuits*, 5th ed. New York: John Wiley and Sons, Inc., 2009, pp. 5-6.

[13] H. C. Poon and H. K. Gummel. "Modeling of emitter capacitance," *Proc. IEEE*, Vol. 57, pp. 2181-2182, Dec. 1969.

[14] D. Johnsson, private communication, High Powered Pulse Instruments, May 2012.

[15] D. Pogany et al., "Nonlinear dynamics approach in modeling of the onstate-spreading — Related voltage and current transients in 90nm CMOS silicon controlled rectifiers," in *IEDM Tech. Dig*., 2009, pp. 509–512.

[16] R. Mertens and E. Rosenbaum, "Separating SCR and trigger circuit related overshoot in SCR-based ESD protection circuits" in *Proc. EOS/ESD Symp*., 2013.

[17] C. Russ et al., "GGSCRs: GGNMOS triggered silicon controlled rectifiers for ESD protection in deep sub-micron CMOS processes," in *Proc. EOS/ESD Symp*., 2001, pp. 22-31.

[18] D. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: John Wiley & Sons, Inc., 1998, p. 217.

[19] T. J. Maloney, "Evaluating TLP transients and HBM waveforms," in *Proc. EOS/ESD Symp.*, 2009, pp. 143-151.